Docket No.: S&ZIO020103

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : ASTRID ELBE ET AL.

Filed : CONCURRENTLY HEREWITH

Title : METHOD AND APPARATUS FOR MODULAR MULTIPLYING
AND CALCULATING UNIT FOR MODULAR MULTIPLYING

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

S i r :

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications
are submitted herewith:

German Published Non-Prosecuted Patent Application DE 36 31 992 A1 (Sedlak),
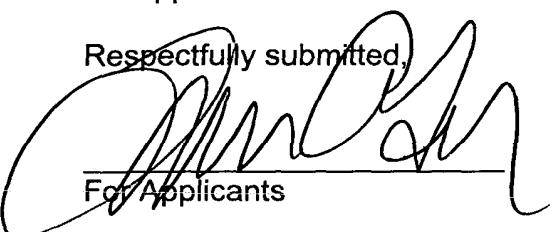dated November 5, 1987 and English abstract thereof;

PCT WO 00/38047 (Glaser et. al.), dated June 29, 2000;

Drescher, W. et al.: "VLSI Architectures for Multiplication in GF (2^m) for Application
Tailored Digital Signal Processors", IEEE, 1996, pp. 55-64;

Orton, G. A. et al.: "VLSI Implementation of Public-Key Encryption Algorithms",
edited by G. Goos and J. Hartmanis, Lecture Notes in Computer Science, Advances
in Cryptotology-CRYPTO '86, Springer-Verlag, pp. 277-301.

If no translation of pertinent portions of any foreign language patents or publications
mentioned above is included with the aforementioned copies of those applications,
patents and/or publications, it is because no existing translation is readily available to
the applicant.

Respectfully submitted,

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For Applicants

Date: July 21, 2003

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FORM PTO-1449 (SUBSTITUTE)	Attorney Docket No.: S&ZIO020103
U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	Appl. No.:
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (37 CFR 1.98(b))	Applicant: ASTRID ELBE ET AL.
	Filing Date: July 21, 2003 Group Art Unit:

EXAMINER INITIALS		PATENT NO.	DATE	PATENTEE	CLASS	SUB CLASS	FILING DATE
	A						
	B						
	C						
	D						
	E						
	F						
	G						
	H						
	I						

FOREIGN PATENT DOCUMENT

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB CLASS	TRANSL. YES	NO	
	J	36 31 992 A1	11/5/87	Germany				
	K	00/38047	6/29/00	WIPO				
	L							
	M							
	N							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

		Drescher, W. et al.: "VLSI Architectures for Multiplication in GF (2^m) for Application Tailored Digital Signal Processors", IEEE, 1996, pp. 55-64
		Orton, G. A. et al.: "VLSI Implementation of Public-Key Encryption Algorithms", edited by G. Goos and J. Hartmanis, Lecture Notes in Computer Science, Advances in Cryptotology-CRYPTO '86, Springer-Verlag, pp. 277-301

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.